Design for Manufacturibity
The impact on the Physical Design Stage and flow

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Abstract

In this paper I present the impact of sub-wavelength optical lithography for new EDA tools, IC Layout Design flows and manufacturability. We discuss the necessity of corrections for optical process effects (optical proximity correction (OPC) and phase-shifting masks (PSM)) and will focus on the implications of OPC and PSM for layout design and verification methodologies. Our discussion addresses the necessary changes in the design-to-manufacturing flow, including infrastructure development in the mask and process communities as well as opportunities for research and development in IC physical layout and verification stage.

Reticle enhancement technologies (RET) like optical proximity correction (OPC) and phase shift masking (PSM) have significantly increased the cost and complexity of sub-micron nanometer photomasks. The photomask layout is no longer an exact replica of the design layout. As a result, reliably verifying RET synthesis accuracy, structural integrity, and conformance to mask fabrication rules are crucial for the manufacture of nanometer regime VLSI designs. New EDA systems were recently developed consists of efficient wafer-patterning simulators that is able to solve the process physical equations for optical imaging, resist development and hence can achieve high degree accuracy required by mask verification tasks. These tools are able to efficiently evaluate mask performance by simulating edge displacement errors between wafer image and the intended layout. I'll discuss the capabilities for hot spot detection, line width variation analysis, and process window prediction capabilities with a sample practical layout. I'll also elaborate the potential of the new physical model simulator for improving circuit performance in physical layout synthesis.

1. Introduction

Reticle enhancement technologies for VDSM (Very Deep Sub Micron) integrated circuit manufacturing has dramatically complicated the mask data and increased the cost of advanced photomasks. The increase in pattern complexity due to optical proximity correction (OPC), the tight requirements for Critical Dimension (CD) control, and the difficulties in defect inspection and repair all contribute to the manufacturing cost increase. For phase shift masks (PSM), the problems are compounded by additional requirements such as controlling the etching of multiple materials, alignment of multiple layers, and inspecting small defect with weak signals. In addition to the added complexities in mask making, the growing array of Reticle Enhancement Technologies (RET) also put more constraints on the physical layout design and verification as physical layouts must be RET compliant and conform to the mask fabrication rules. For instance, the avoidance of phase conflicts in alternating PSM and generating OPC-friendly design layout are examples of those new constraints. Physical design and verification flow nowadays have to be overhauled to address various wafers and photomasks manufacturing issues explicitly early in the design flow to achieve high quality fabricated silicon at a reasonable point on the price-performance curve. There are tremendous amount of research efforts from the industry and academia for this issue.

The complexities in mask data and manufacturing make it highly desirable to verify and optimize the mask data independently before committing to the costly fabrication process. An effective method for post-RET mask data verification is to simulate its image on the silicon wafer and compare it with the original design intent. This method places mask data in its intended operating environment and evaluate its performance metrics that have direct impact on wafer imaging. A simulation based verification system can evaluate the process for a product and give warning on certain performance limiting spots on the layout and thus significantly reduce the risk of mask data errors. Once the troubling spots are identified, localized corrections can be applied to extend the process window in an intelligent way.

The existing model based mask layout verification systems have a few areas that require further improvement. First, they are typically implemented with the same simulation engine with model based OPC. Sharing the simulation engine with OPC, the verification also inherits the errors of the OPC model. The logical dependency jeopardizes the probability of finding OPC errors, and reduces the reliability of the verification. A process window is the range of process parameter variations under which the line width remains within limits Secondly; they employ empirical modeling approaches that cannot easily track acceptable variations in process conditions. In order to sample a different condition in the process window, a different set of models has to be developed, which consumes significant effort and time.
In addition, there is no inherent reason why one set empirical models can judge the result of another if they are derived from the same set of mathematical formulation and training patterns. A full-featured photolithography simulator for mask data verification has been developed for the past decade by the major EDA vendors. (Mentor Graphics, Cadence) This type of simulators have been used extensively in lithography process development where they have demonstrated high accuracy for process predictions.
A mask data verification flow around the physical lithography simulation core that is independent from the OPC engine, thus free from the logical dependency between OPC and its verification. The use of physical models opens the possibility for achieving higher prediction accuracy on complex layout configurations. In addition, physical model can naturally predict the pattern transfer behavior under process variations such as focus change. Furthermore, a physical layout design can efficiently leverage this physical model simulator to improve circuit performance and reduce the manufacturing variations.

2. Physical Model Based Mask Layout Verification Flow

A standard flow for reticle enhancement and optical proximity correction with model based mask data verification block outlined with gray shading is shown in Figure 1. Here we consider model based OPC as an independent module because it is also needed for all other reticle enhancement techniques as well as standard binary masks. The main manufacturing flow is shown on the left hand side. The design layout from a customer is modified with reticle enhancement, followed by model based OPC to produce a set of mask geometry data that is suitable for mask manufacturing. The model generation flow is shown on the right, where a test layout is printed with the same pattern transfer process to produce an experimental data set for empirical model fitting. The resulting model can then be used in the OPC engine to predict the wafer CD error. From that, the amount of mask correction can be calculated.

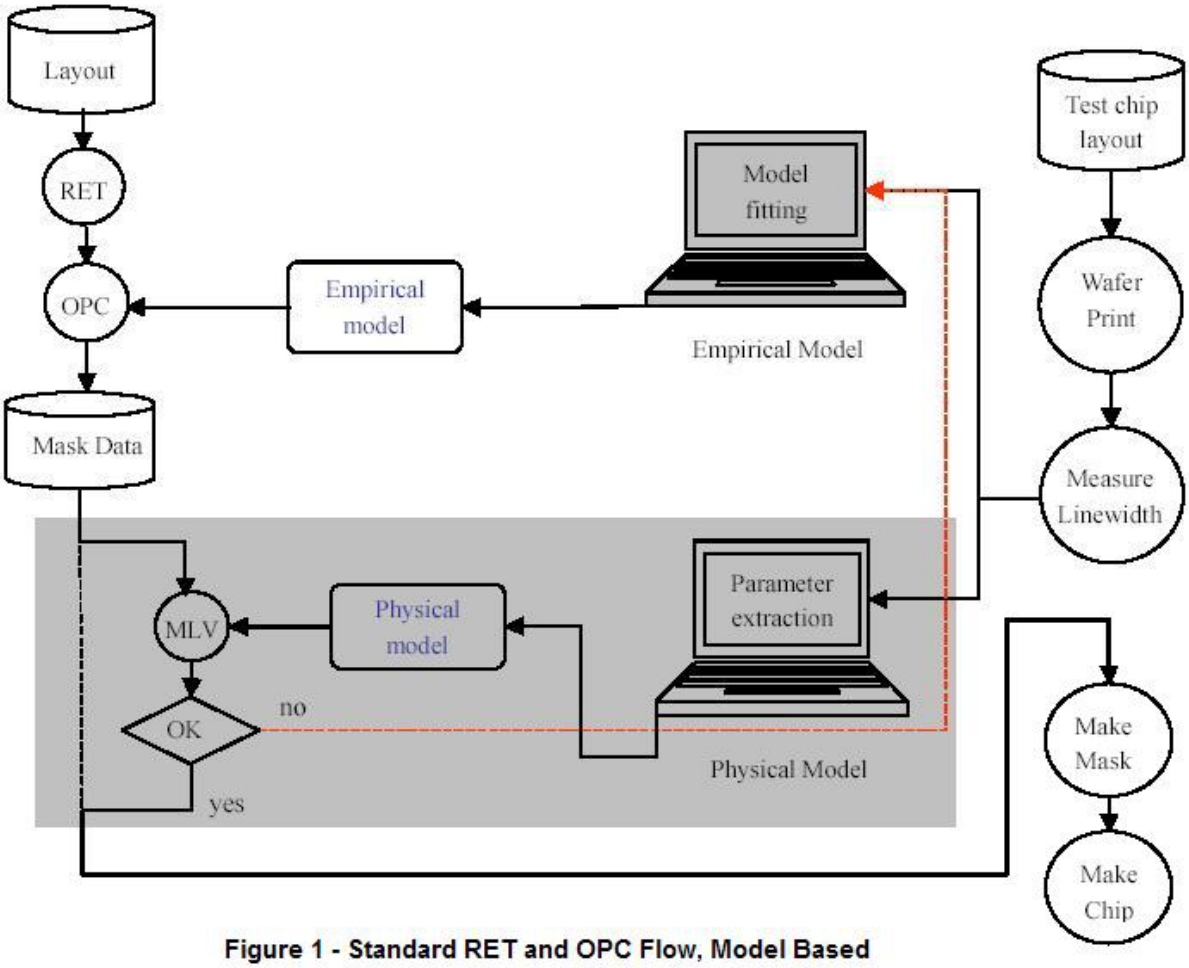

Figure 1 - Standard RET and OPC Flow, Model Based

To implement physical model based mask data verification, one must calibrate the physical model by extracting the process parameters from the same data set used for empirical model fitting. The main task here is to obtain resist-processing parameters such as development rate parameters and the post exposure bake diffusion length.
The model can then be used in the mask layout verification (MLV) block to check the post-OPC mask data.

The verification can be performed on the entire mask or, to save processing time, on sections of the mask that are most likely to have pattern transfer problems. In case such problems are found, the simulation pattern produced by the physical model and the corresponding mask section can be added to the data set for recalibrating the empirical model. This feed back system will gradually make the empirical model to become more predictive over time as more and more cases are added to the training set. At some point, the confidence level on the empirical model will reach a point when only occasional verification is needed in the full production mode.

A detailed Physical Model based mask verification (PM-MLV) block is sown in Figure 2. The intended layout is derived from the design data by applying appropriate geometry operations such as scaling and sizing. This design intent is used as the standard for comparison. The other path of the verification process takes the mask layout as input and run through the wafer - patterning simulator. It simulates the wafer pattern by solving the equations describing image formation, resist exposure, post exposure bake, development and etching.
The simulation parameters are set such that the resist and etching processes are accurately captured in the model. By doing so, any changes on the RET type, exposure tools settings, and thin film stack can be predicted by the physical simulator.
The output of the high accuracy wafer-patterning simulator is the outline of wafer image. The pattern differentiator in Figure 2 compares this with the design intent and outputs the difference between the two patterns. The system characterizes the pattern difference by calculating the displacement of a line segment on the intended layout to its counterpart on the wafer image.

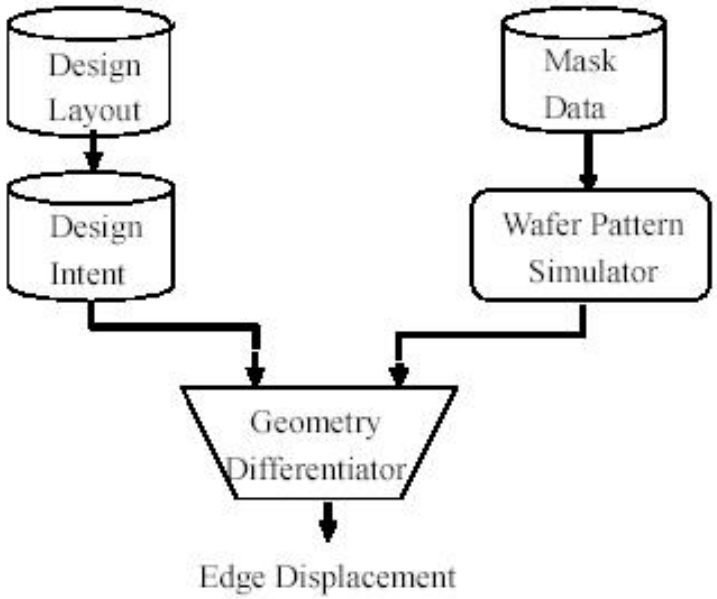

Figure 2 - Detailed PM-MLV

Positive edge displacement indicates that the wafer pattern falls outside the original design polygon, and is larger than the design intent. Similarly, a negative edge displacement indicates that wafer pattern is smaller than the design intent. In order to better capture the variations along a polygon edge, the edges of the design intent polygons are subdivided into shorter segments for edge displacement calculation. The subdivided edge segments are classified in a feature specific way in the data representing the design intent. For example, the segment located on a line end will carry a special flag indicating that line end pull back will be measured for this segment. Similarly, segments at long line edge may carry another flag indicating that transistor gate or local interconnect variations will be measured at these segments. The feature specific classification flags help a user to impose different verification tolerance for each feature class of edges. By doing so, the verification process can be customized to better reflect the yield and performance of the product.

3. Hotspot Detection

Processing hotspots are the locations in the design where the magnitude of edge displacement is exceptionally large. Hotspots can form under a variety of conditions such as the original design being unfriendly to the RET that is applied to this chip, unanticipated pattern combinations in rule based OPC, or inaccuracies in model based OPC. When these hotspots fall on locations that is critical to the electrical performance of a device, they can reduce the yield and performance of the device.

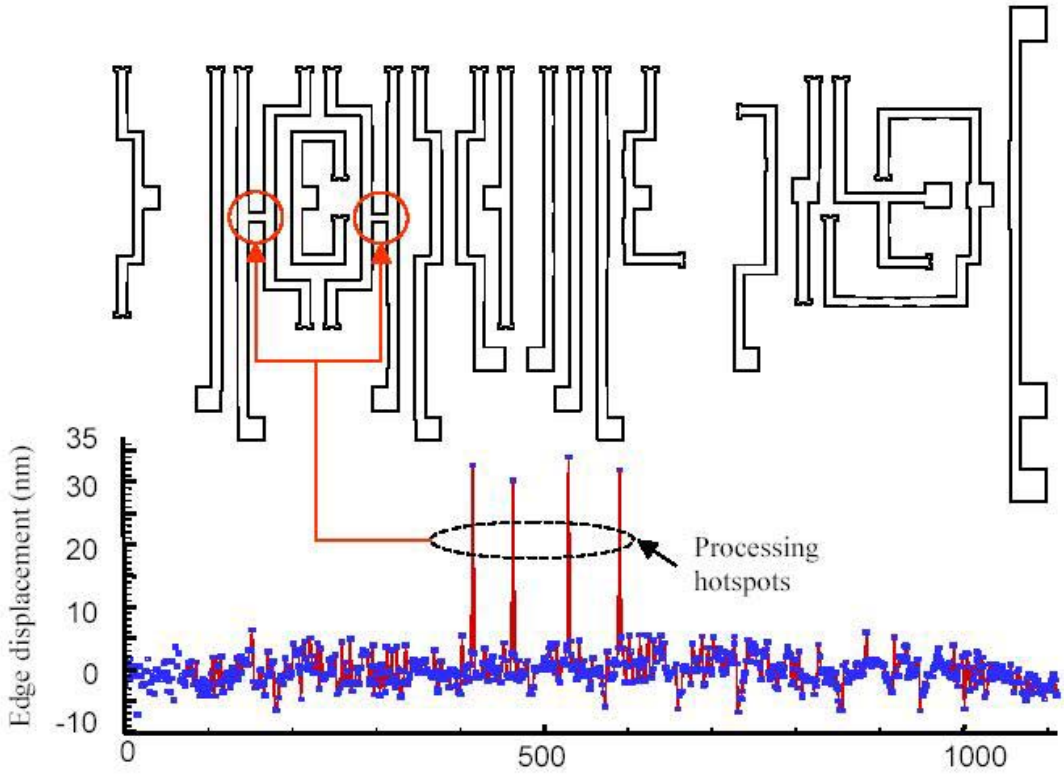

Figure 3 – Hot Spots Detection

Physical model based mask layout verification (PMMLV) can identify the hot spots and subsequently repair them by applying physical model based OPC (PM-OPC) at these locations. (Shown on Figure 3) The layout is for the poly gate layer with 90 nm target line width and dominating pitch of 300 nm. The cell size is approximately 11 um by 6.6 um. The mask layout is created by model based OPC using aerial image model only.

After OPC, the standard deviation of edge displacement error is calculated to be 0.71 nm, which confirms that the wafer pattern as predicted by the aerial image simulation is in good agreement with the design intent. The performance of this OPC mask created with simple aerial image model is verified using an optimized isofocal2 resist recipe that is a more realistic description of the patterning process. Also shown in Figure 3 is the output of the pattern differentiator. The edge displacements are evaluated on 887 line segments on this cell.

Our PMMLV process discovers four segments with large edge displacement as shown in Figure 3. Interactive exploration shows that these points are located on either side of the short horizontal bars in "H" shaped patterns. The standard deviation for edge displacement also increased 240% from 0.71 nm to 1.7 nm. This set of verification result shows that the mask data created by OPC with simple aerial image model would result in worse process and circuit performance than that suggested by the small correction residual.

4. Proximity Induced Line Width Variation Statistics

Variations in line width due to lithography and etching often limit the performance of a circuit. The line width variation pattern changes as focus varies within allowed process control limits. Existing OPC methodology is aimed at reducing the line width variability at a nominal focus point, without considering the potential impact of focus change.

In this case, physical model can be applied to obtain more complete and meaningful line width variation statistics by considering focus and other process parameter variations, the result of which can be used for performance optimization.

Figure 4 show the histogram for the edge displacement under defocus for a mask produced by physical model based OPC. At best focus, the mean edge displacement is zero, indicating an on-target CD distribution at 90 nm. The standard deviation of the edge displacement is 0.97 nm, which represents the residual of PM-OPC process. When this mask is printed under 0.15 um of defocus, the distribution broadens into a bi-modal form. We can clearly see the increase in the edge displacement envelope under defocus.

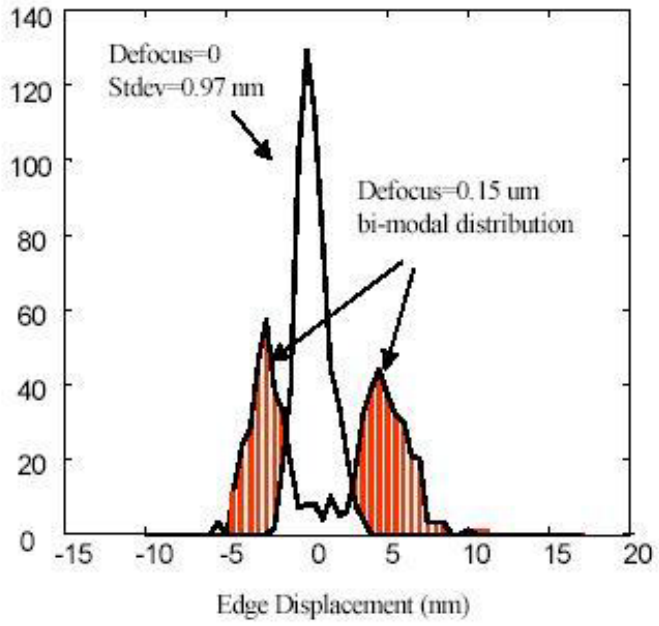

Figure 4 - Edge Displacement Error

The mean of the edge displacement, however, still stays at near zero, as in the best focus case. On average, the line width is not changed under defocus, as the number of edges with positive displacement roughly equals the number of edges with negative edge displacement. This behavior is consistent with the isofocal process model we developed for this circuit. On the other hand, if the same circuit layout is corrected with aerial image model and verified using aerial image model, a -14 nm average edge displacement will result with 0.15 um defocus. The range of variation also increases by nearly a factor of 7 from 0.71 to 3.5nm. The large difference in response between this and physical model based OPC and verification shows the strong influence of models on the OPC and verification results.
The edge displacement statistics produced by the physical model based OPC and verification process can be used in physical design flow to make ECAD tools manufacturability aware such that process variations can be reduced and circuit performance can be improved. This concept is illustrated in the following section.

5. Impacts on Physical Design Stage and Flows

The circuit design and mask processing are still basically separated from each other in current design and manufacturing flow. The design and process development team communicate only through a set of design rules. As we moving into VDSM technologies, we have to explicitly addressing various manufacturing issues early in the physical design flow to attain the best design performance, process window and uniformity in manufacture. Recent approach to this change in design-manufacturing interaction is through advanced process simulation that is transparent to circuit designers.
Figure 5 shows recent mode of design-process interaction. For each new technology node, the equipment community publishes tool specifications early in the process development cycle. These parameters are used to construct physical models well before an intended process becomes stable. These physical models are applied early in the design phase to ensure that the layout can be optimized for the target processing technology.

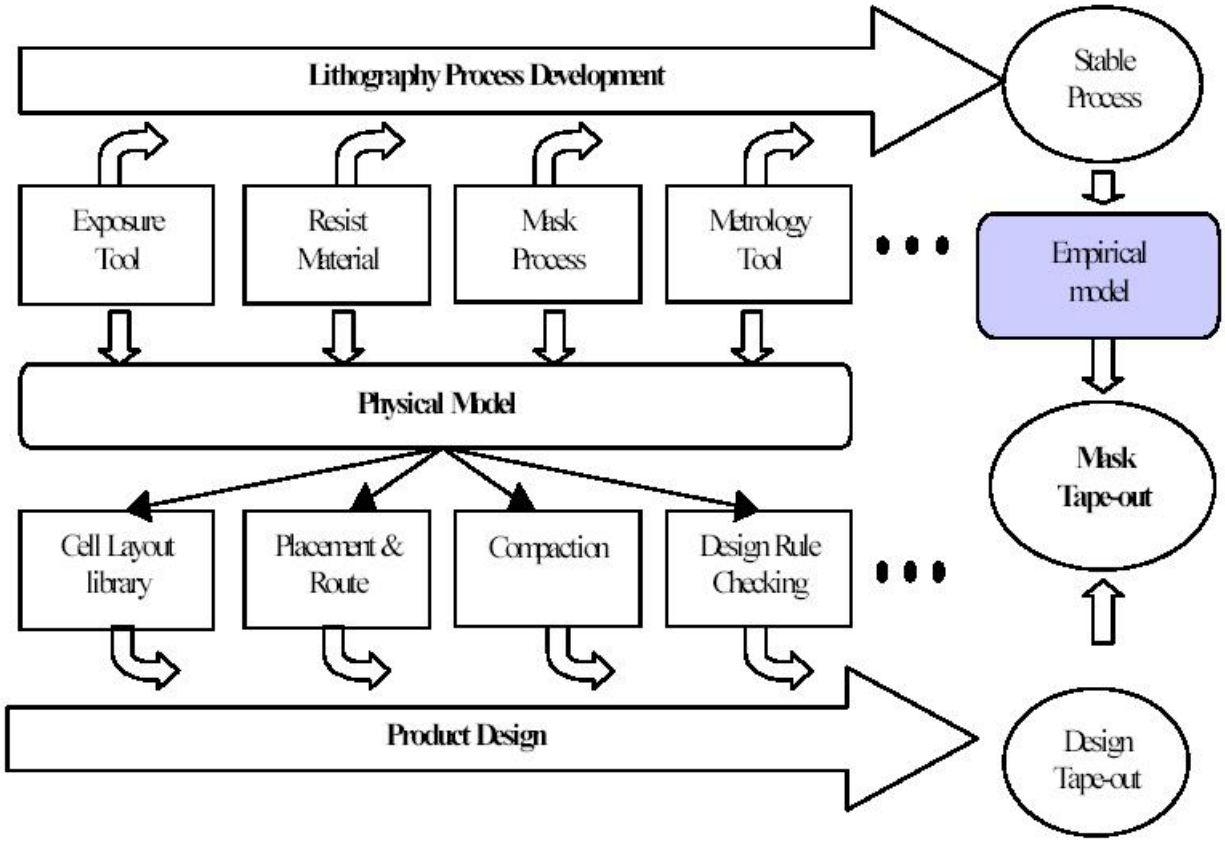

Figure 5 - Recent Design and Process Flow

Manufacturing information such as process variations of channel lengths (channel edge displacement) and local interconnect variation under different RET configurations are used to guide physical design to reach the best point on the performance-cost curve.
The key advantage of a physical model is that it does not depend on training patterns from a mature process. So it allows design library to be created in parallel with the process development. As a result, we can compute all the performance statistics like static/dynamic power consumption and delay for each OPC-processed cell in the library.

Now designers can pre-characterize OPC related information for each cell and use this information during placement to produce more OPC-friendly layouts. Specifically, we need to know how sensitive (*sensitive factor*) the critical dimensions (CDs) in a cell to its neighborhood patterns and how difficult to compensate the CDs in the cell. If an aggressive OPC is needed (like sub-resolution assistant features which may be outside of original cell layout), then the cell layout area has to be bloated. Now we can build different *OPC configurations* for each cell in the library, each of them has different layout area and OPC performance in terms of statistic errors on CDs.

6. **Power Leakage**

In the following, I'll show how different OPC configurations can affect the power leakage of a CMOS device. Static power leakage becomes a major concern for designers today, as it accounts for an increasing and significant portion of the total power budget in high-end microprocessors. This situation will become even worse with further reduction of threshold voltage (Vth) of MOS devices. CMOS device leakage currents I_{sub} varies exponentially with the change of channel length *L* as shown in the formula below:

$$I_{sub} = K(1/L)\exp(-CL)$$

where *K* and *C* are device dependent constants. As a result, the sub-threshold leakage currents are extremely sensitive to the channel length variations. The mean leakage current of a chip under process variations can deviate significantly from the nominal leakage current in a typical 0.18 um COMS process. The mean leakage current and the standard deviation of a PMOS transistor vary with the changes of its channel lengths due to different OPC configurations. The process used here is TSMC high-performance 0.13 um technology. Table 1 shows our calculated mean leakage and standard deviation of mean leakage of sub-threshold current of PMOS device under different OPC configurations.

OPC Cfg	Stdev. of L σ (nm)	% Variation (3σ)	Mean Isub (nA)	Stdev. Of Isub (nA)
Phy-Model OPC	0.5	1.8%	4.0205	0.48
Std. OPC	2	7.5%	4.4661	1.88
No OPC	5	18.8%	6.9614	3.84

Table 1 - Leakage Current Variation - PMOS Device
Channel Length Variation Range: L=0.08 um W/L=5

It is shown that average leakage will significantly deviate from nominal value if no OPC is used. If OPC is employed, but is not optimized due to poor modeling or unexpected presence of neighborhood patterns, the average leakage will still %10 higher than the nominal value. With physical model based OPC and predictable neighborhood patterns, the channel length variation can be well controlled. As a result, the mean leakage current and its variation are reduced. The statistical performance information of library cells can be leveraged during physical layout synthesis. For example, in the detailed placement phase, all the timing critical or leakage cells (called *critical cells* in the sequel), which are also OPC sensitive are instantiated with their best OPC configurations. Placement will legalize the added areas of those cells during refinement. If a cell is no longer a critical cell, its original layout will be used again. For OPC high sensitive critical cells, a fast on-line OPC process can be invoked to estimate the statistic errors for its neighborhood patterns. If the errors are still too large, some local cell swapping may be applied to get different neighborhood patterns or get more open area (adding dummy cells) around the critical cells or even re-synthesis the corresponding logics to make the resulting cell less OPC sensitive.

This process is repeated until OPC CD errors on all the high sensitive critical cells are under control. Such cell-based OPC and the manufacturability-aware placement strategy bring many advantages: First, it will improve the circuit performance and reduce the performance variations and thus unnecessary guard-banding, and lead to much more predictable circuit performances and manufacture yield. Second, with each layout pre-certified and OPC optimized by physical models, the final tape-out process would likely to be much simpler than the whole chip-wide, essentially flattened OPC and verification processes used today.

7. Conclusions

We observed mask data verification flow in order to prevent data problems to propagate to the expensive mask making and wafer printing stage. New flows, presented to the industry by the major EDA vendors leverages the high accuracy of a wafer patterning simulator that predicts the wafer image by solving the equations that describe the physics and chemistry of the pattern transfer process. These systems address the problems of the existing empirical model based OPC/RET flow and can be applied in parallel to improve the reliability and quality of the mask data. We discussed how edge displacement statistical information obtained from the new model simulator can be leveraged during physical synthesis flow to reduce the performance variations and improve the device manufacturability. No Doubt, There is a tremendous impact on the IC Physical Design and verification phase due to the sub-wavelength optical lithography and this will get more critical as progressing towards ultra sub-micron process. EDA vendors are in constant race to implement manufacturability flows for advanced process. In the next decade we will witness a major increase in efforts from industry and academy in the RET arena.

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